

FIG. 1a
(PRIOR ART)

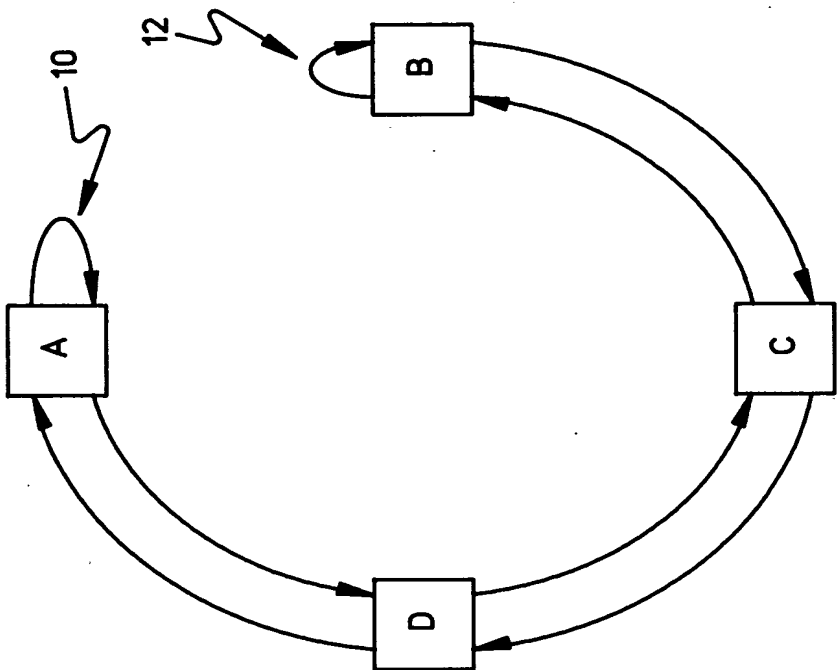


FIG. 1b
(PRIOR ART)

The diagram illustrates the internal architecture of a relay 100, which is a bidirectional communication device. It features four external ports: 1ST INPUT PORT (top left, terminal 102), 1ST OUTPUT PORT (top right, terminal 104), 2ND OUTPUT PORT (bottom left, terminal 108), and 2ND INPUT PORT (bottom right, terminal 106). The internal components and their interconnections are as follows:

- Input/Output Stages:** Each port has a switch (represented by a square with a cross) that directs signals to either the internal processing blocks or the opposite port. For example, the 1ST INPUT PORT switch can route signals to the OCh SYNC CHECK, FEC DECODE, or RE-SYNC FIFO blocks.
- Processing Blocks:**
 - OCh SYNC CHECK:** Located at the top left and bottom right, it performs optical channel synchronization checks.
 - FEC DECODE 110:** Forward Error Correction decoder block on the left side.
 - FEC ENCODE 116:** Forward Error Correction encoder block on the right side.
 - ERR. MON. (Error Monitor):** Receives error signals from the FEC blocks.
 - OH MON. (OH Monitor):** Monitors overhead signals.
 - OH INS. (OH Insertion):** Inserts overhead signals into the data stream.
 - SONET PM (SONET Path Marker):** Manages SONET path markers.
 - RE-SYNC FIFO:** Resynchronization First-In-First-Out buffers on both sides.
 - SW SYS 122:** A central switching system that routes signals between the various processing blocks and ports.
- Buffers and Relays:**
 - SYNC FIFO:** Synchronization First-In-First-Out buffers are located near the top and bottom ports.
 - RELAY 100:** The central switching mechanism that enables bidirectional communication between the ports.
- Signal Flow:** Arrows indicate the direction of data and control signals. For instance, data from the 1ST INPUT PORT can pass through the OCh SYNC CHECK, FEC DECODE, and OH MON. blocks before being routed to the 2ND OUTPUT PORT via the SW SYS 122.

FIG. 2

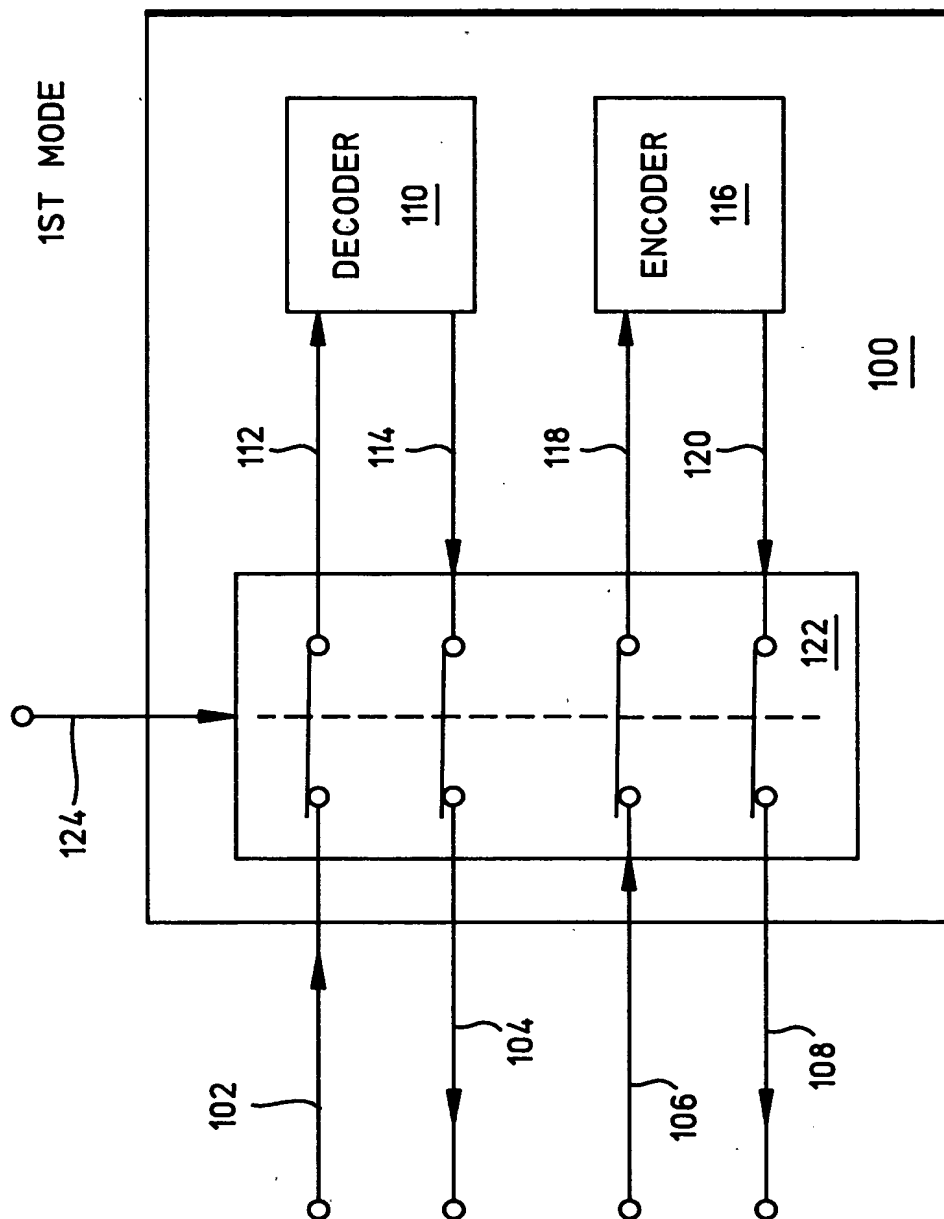


FIG. 3

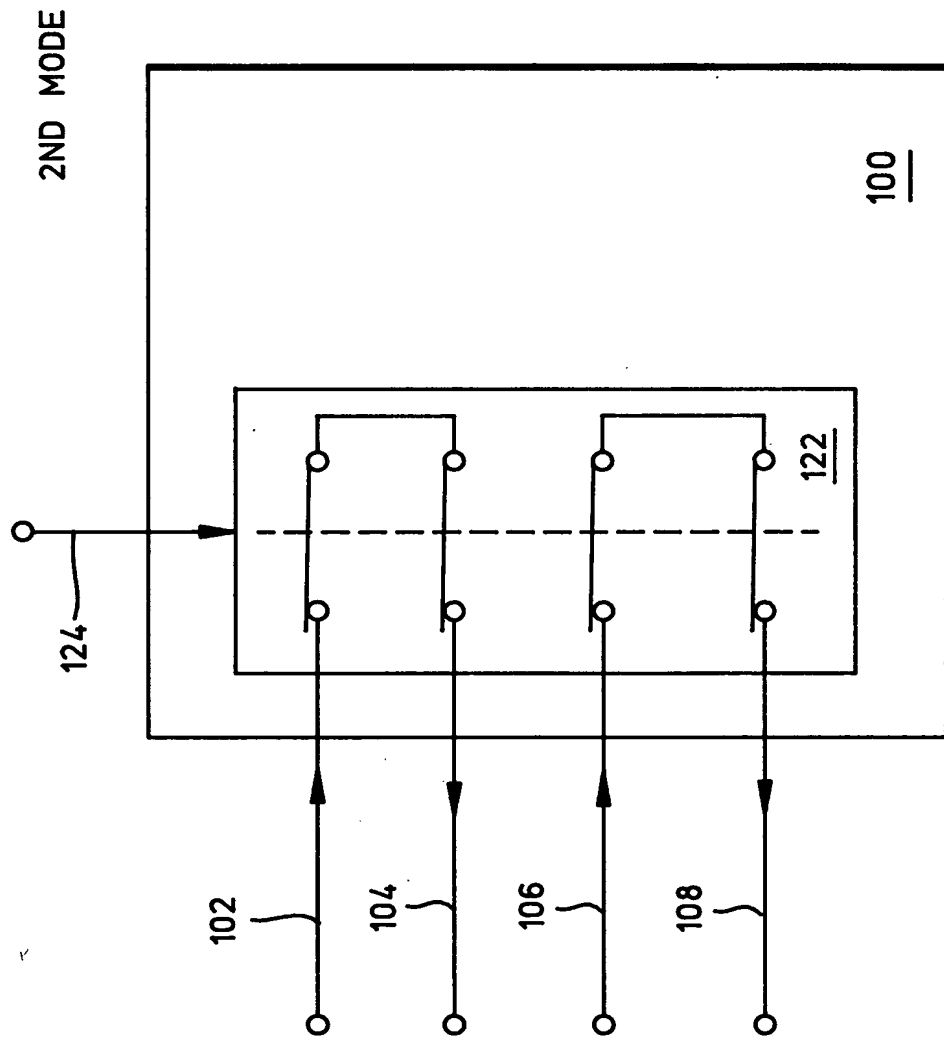


FIG. 4

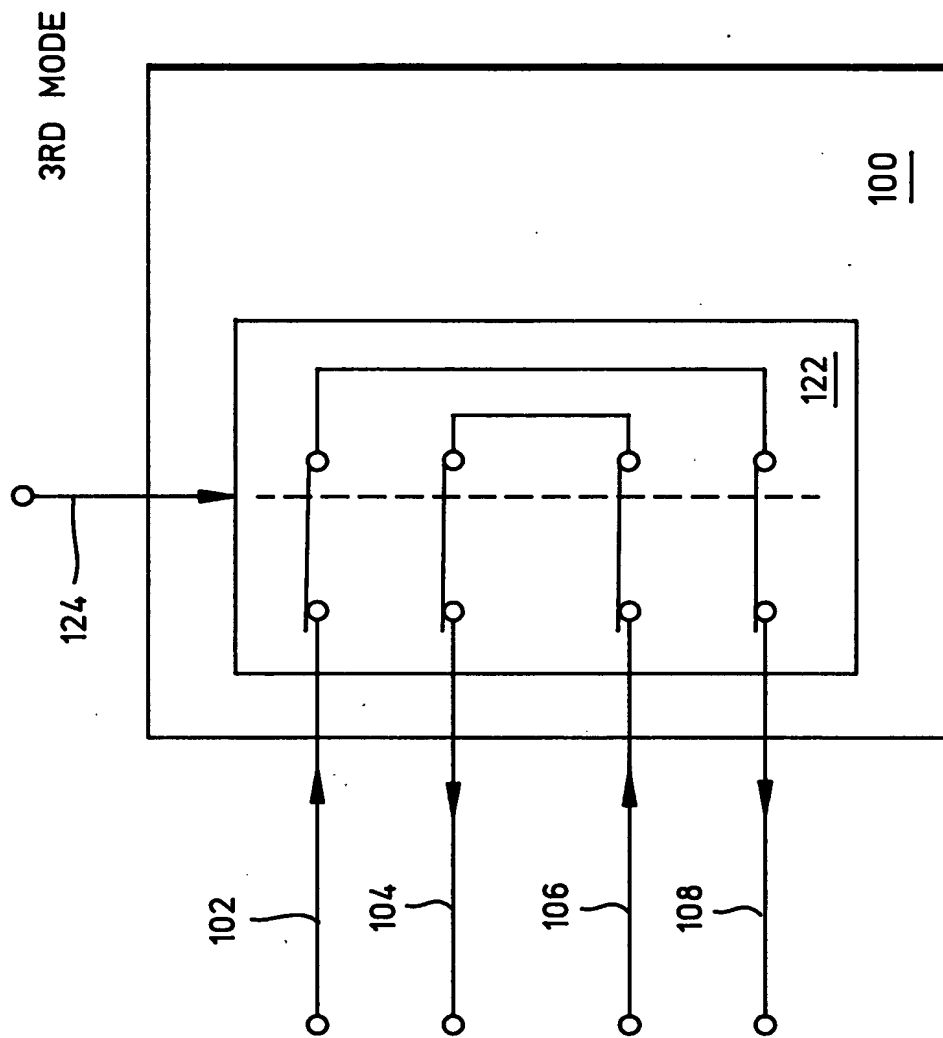


FIG. 5

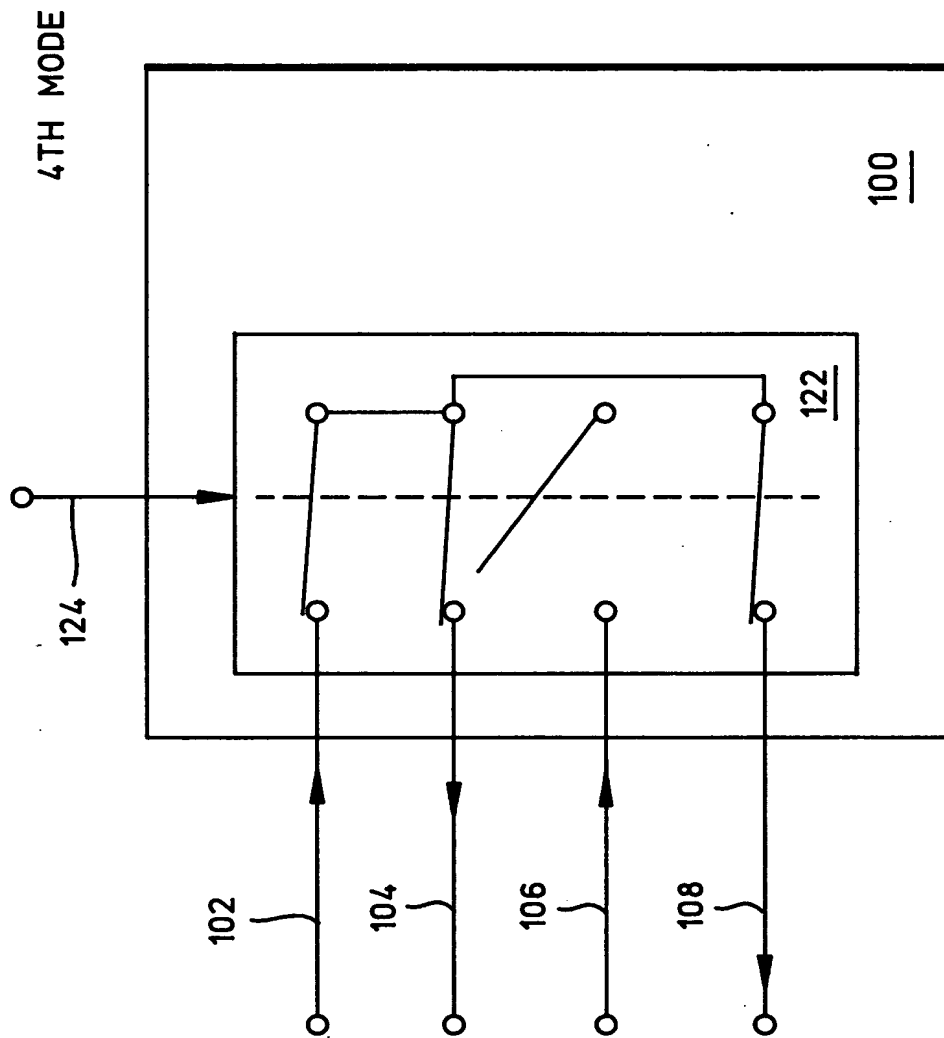


FIG. 6

FIG. 7 is a schematic diagram of a circuit in a 5th mode.

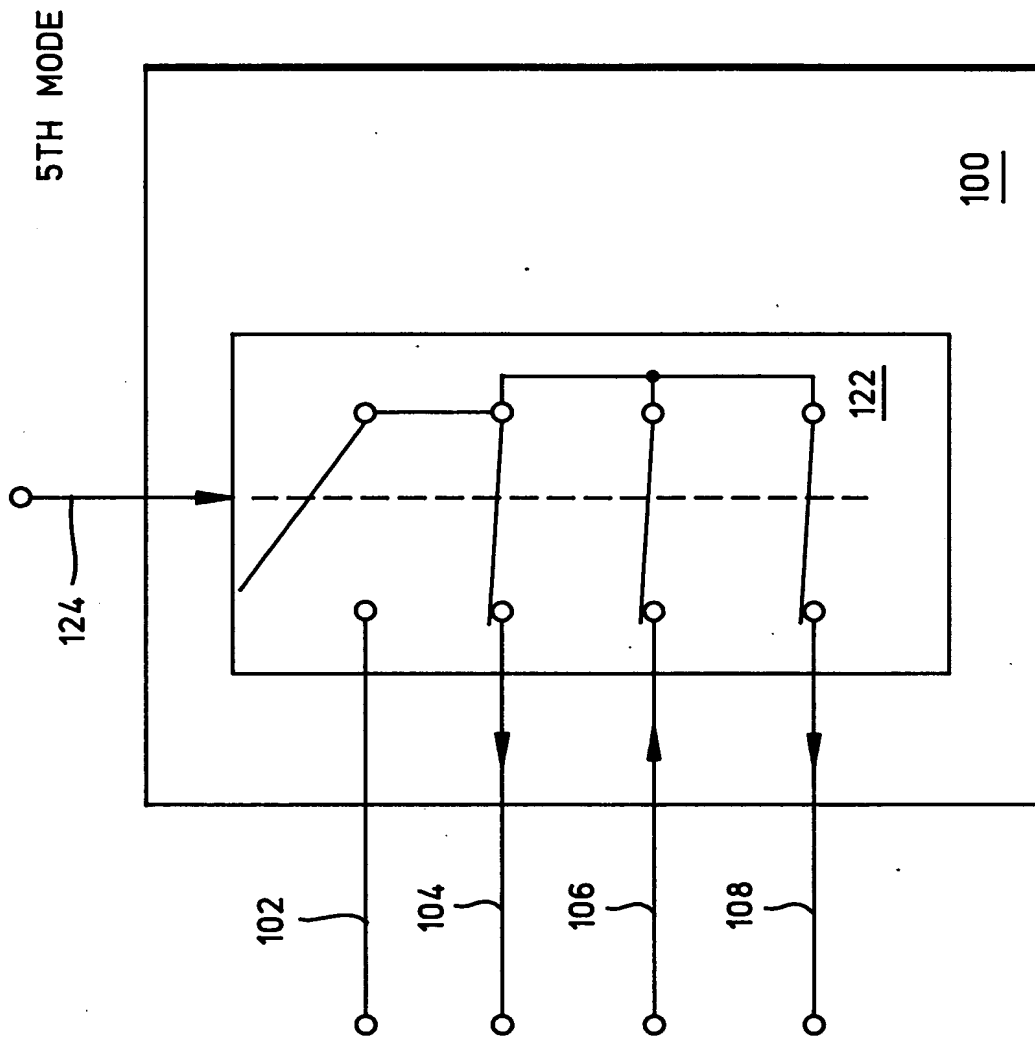


FIG. 7

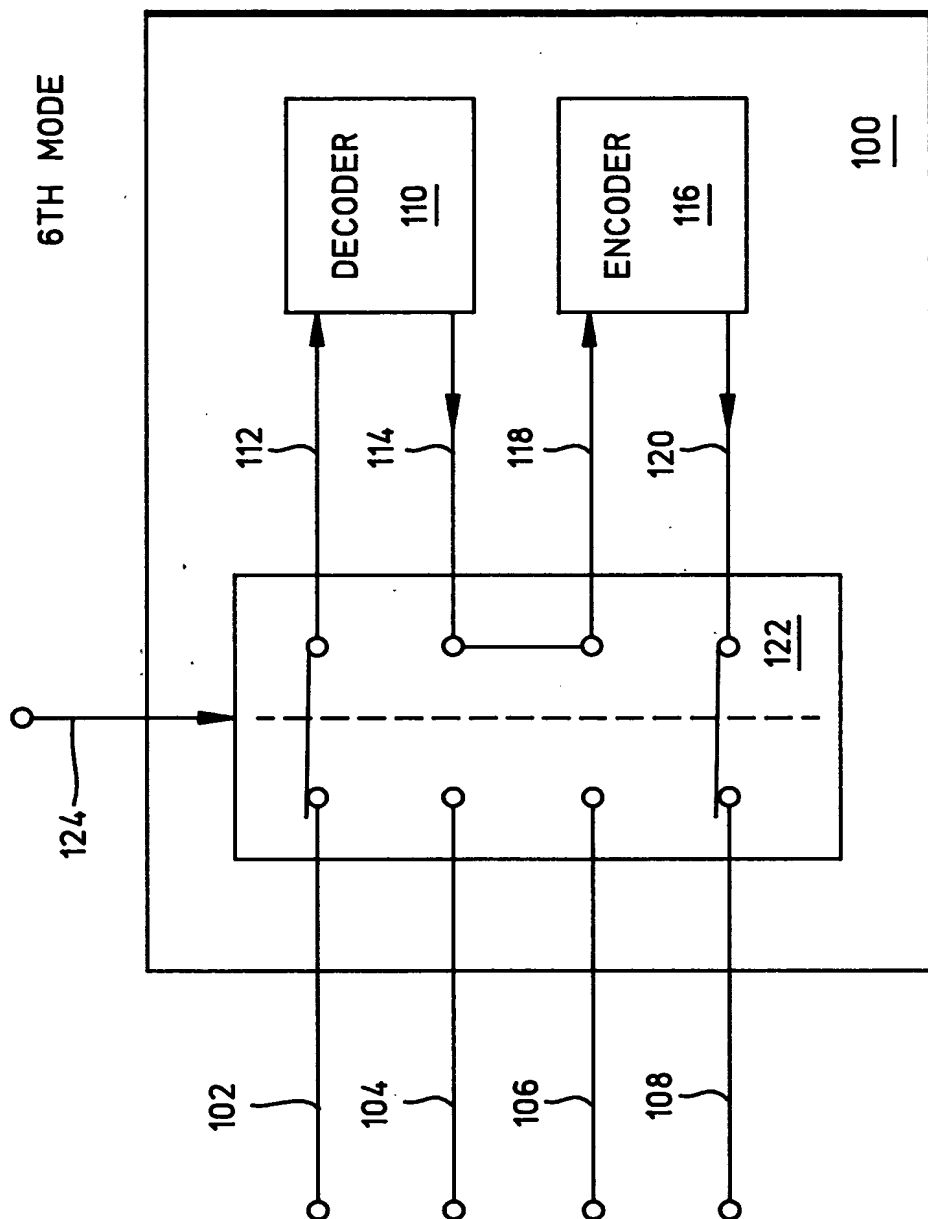


FIG. 8

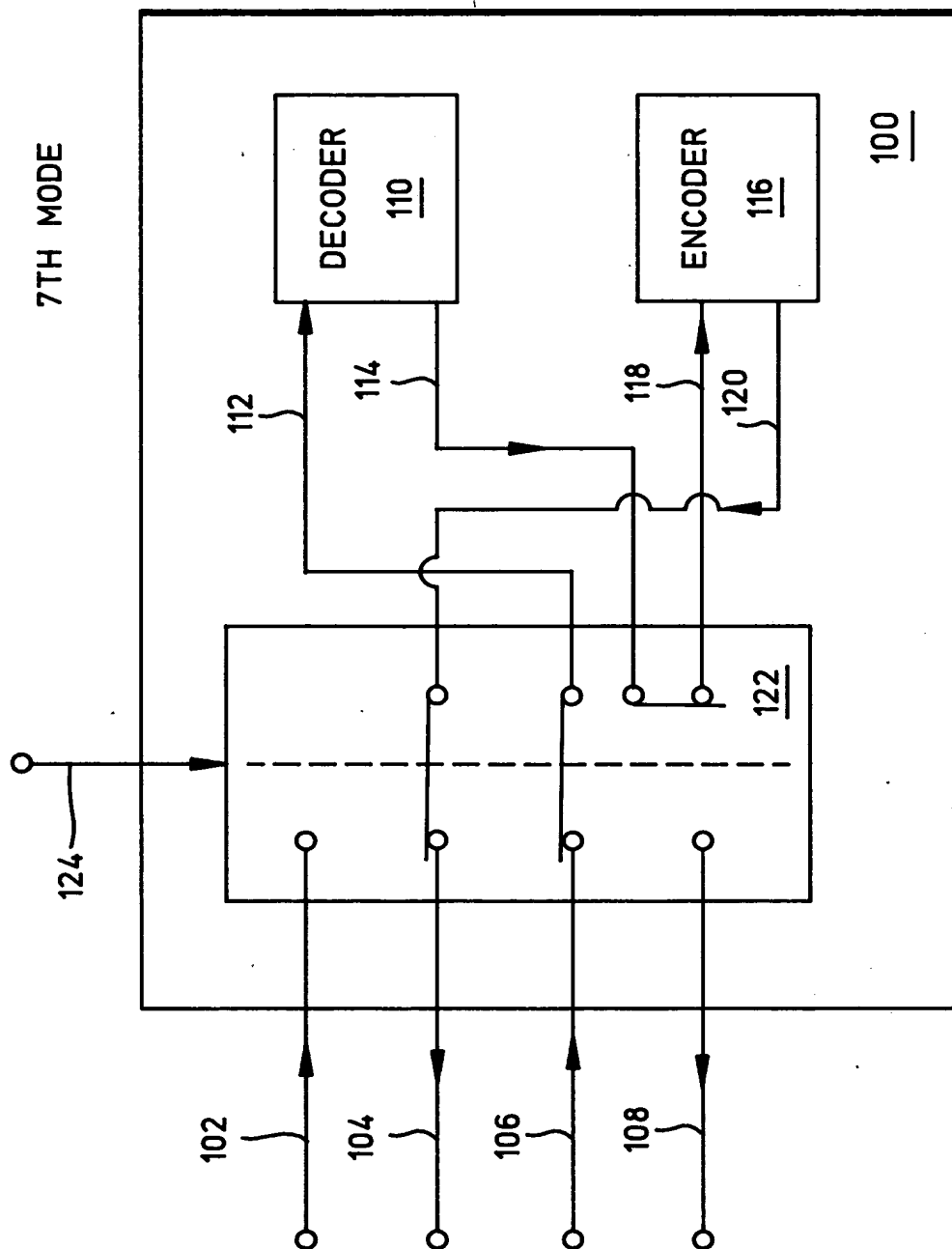


FIG. 9

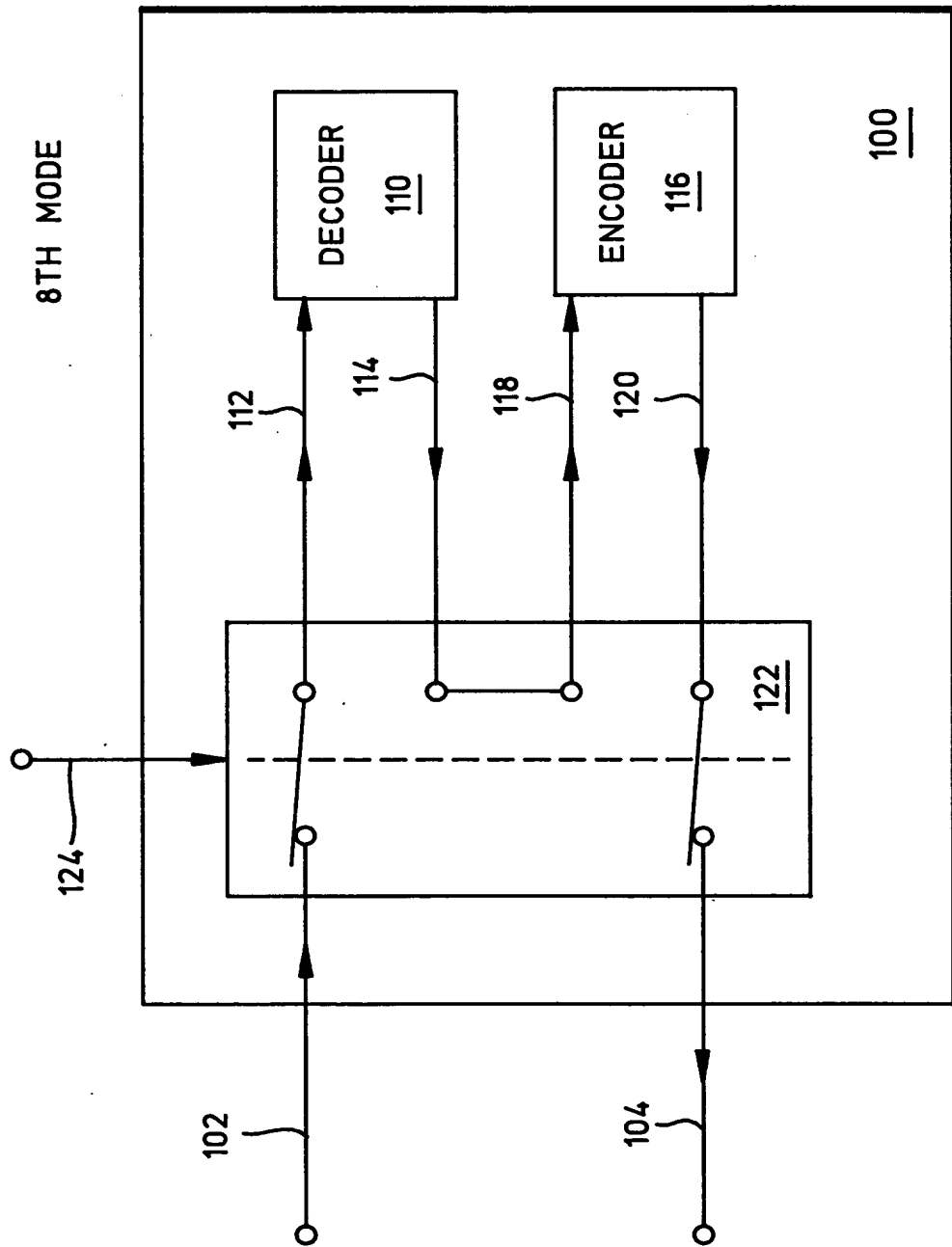


FIG. 10

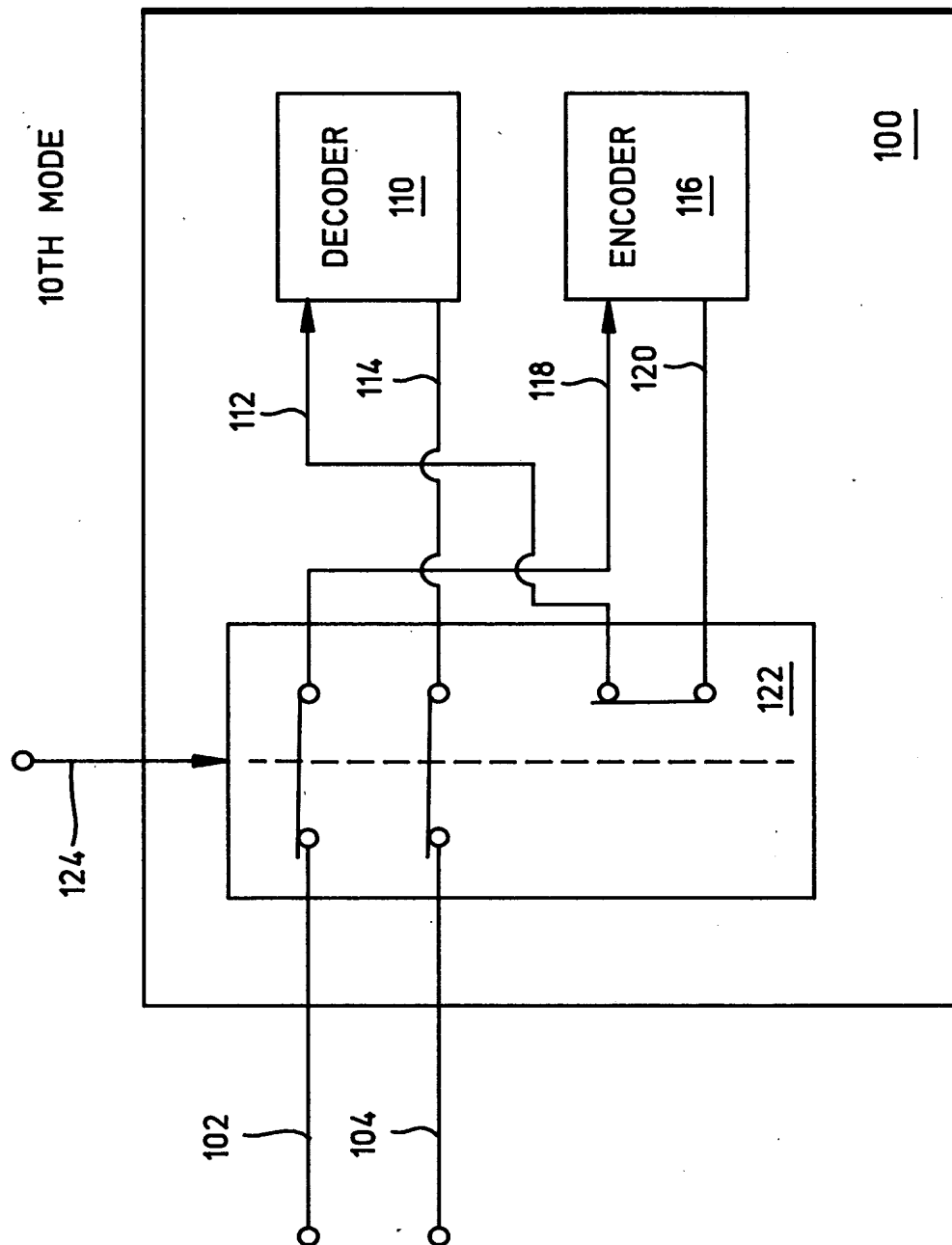


FIG. 11

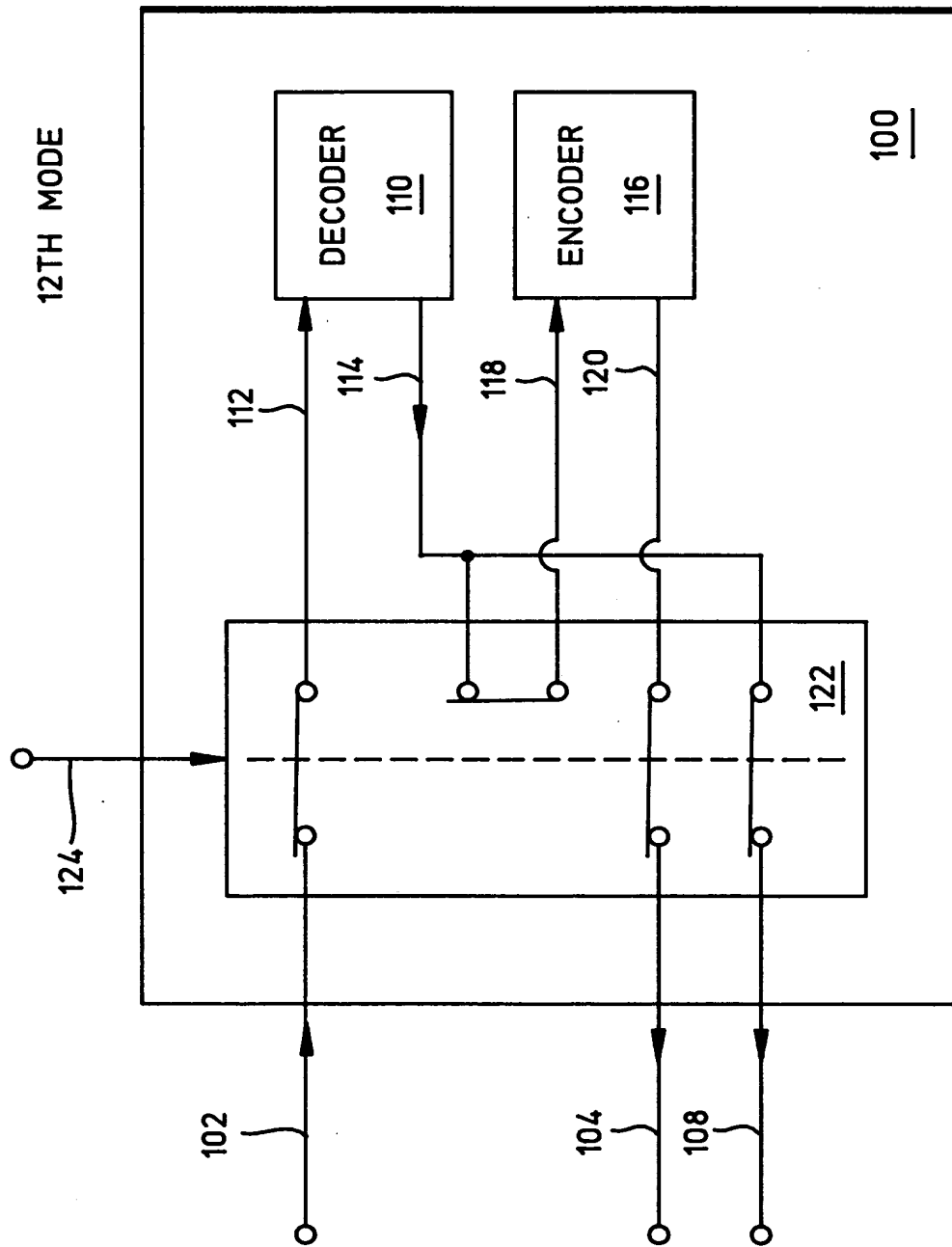


FIG. 12

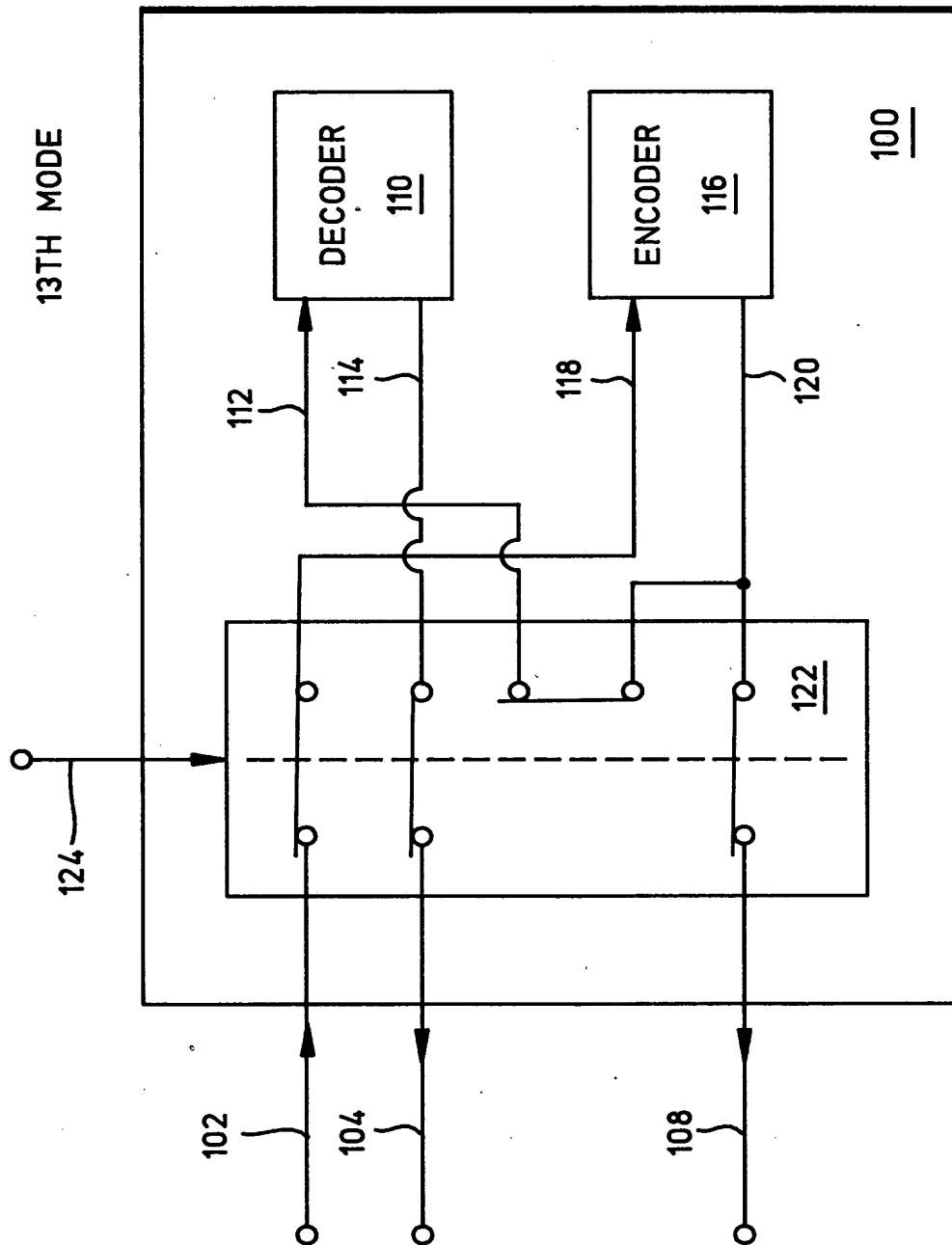


FIG. 13

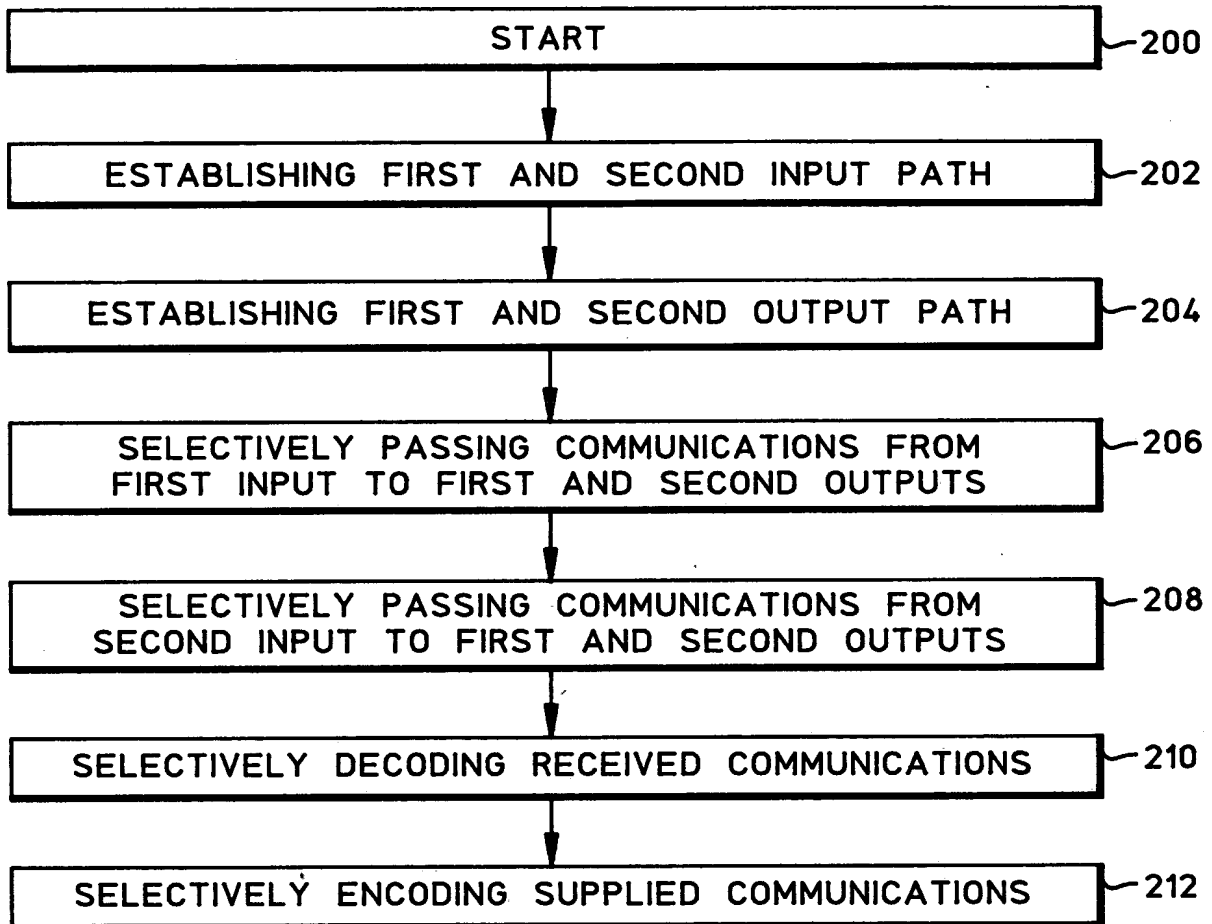


FIG. 14

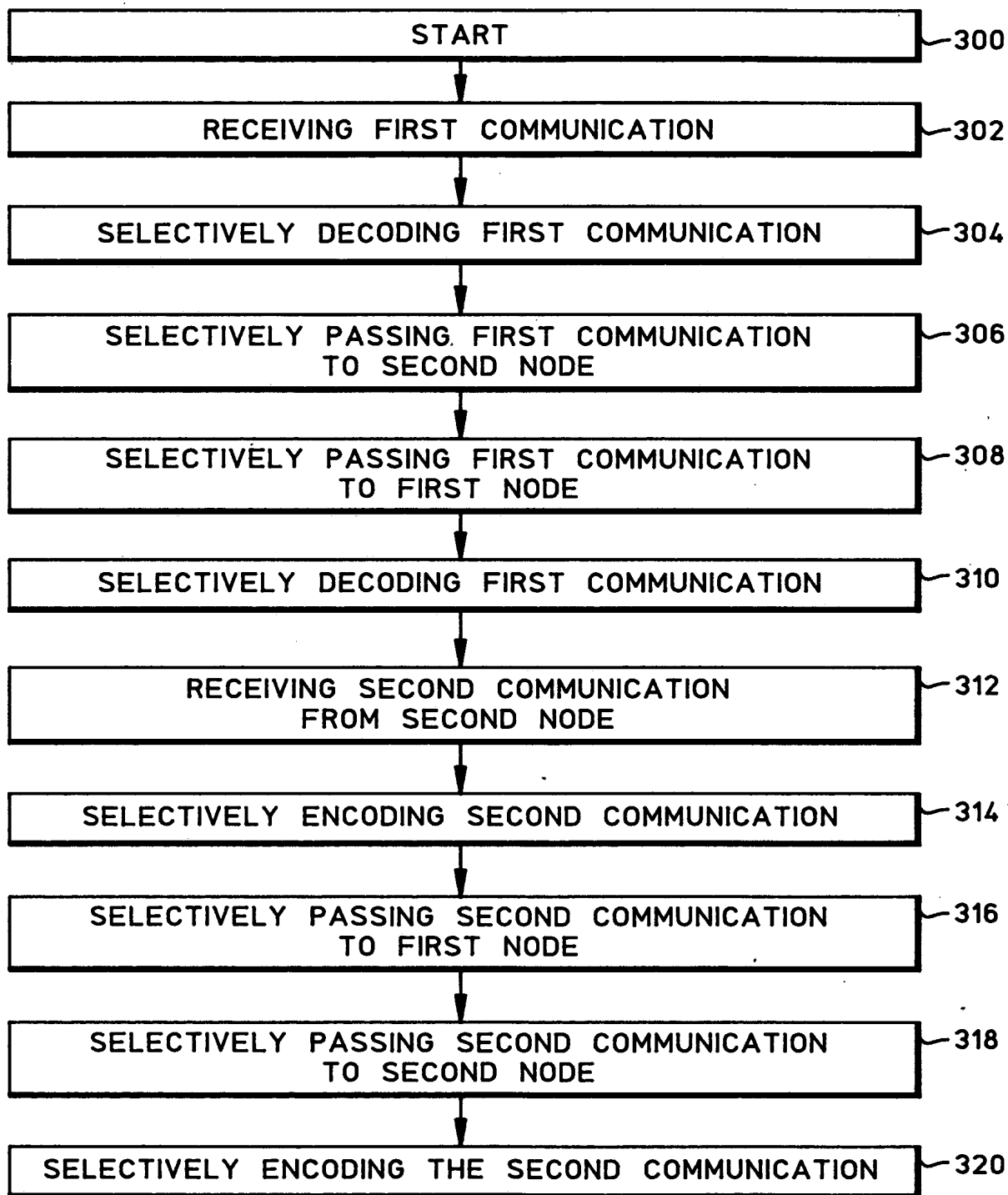


FIG. 15